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(54) **SEMICONDUCTOR DEVICE AND  
ELECTRONIC CONTROL DEVICE**

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**H03M 1/10** (2006.01)

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(2013.01)

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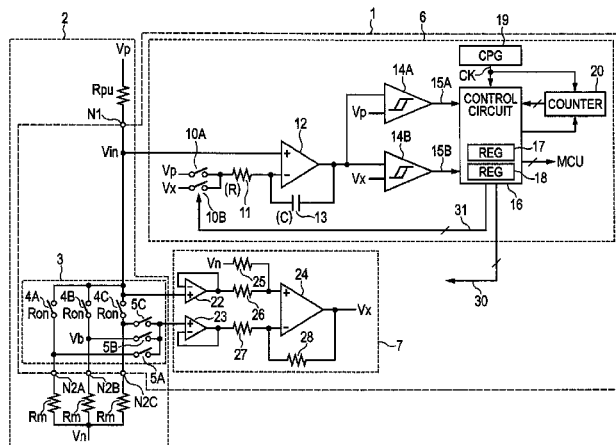
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(57) **ABSTRACT**

To suppress detection accuracy of a measurement resistance  
from decreasing by an on-resistance of a selector switch. The  
selector switch is provided between a first node coupled to a  
first voltage through a reference resistance and multiple sec-  
ond nodes coupled to the second voltage through measure-  
ment resistances, and selects the second node to be coupled to  
the first node with the selector switch. A correction circuit  
generates a voltage obtained by adding the second voltage to  
a voltage between the second node and the first node as a  
correction voltage. A double integral ADC finds a first inte-  
gral time elapsed when a difference voltage of the correction  
voltage to a voltage of the first node is integrated to the first  
voltage and a second integral time elapsed when the differ-  
ence voltage of the first voltage to the voltage of the first node  
is integrated to the correction voltage.

**18 Claims, 11 Drawing Sheets**



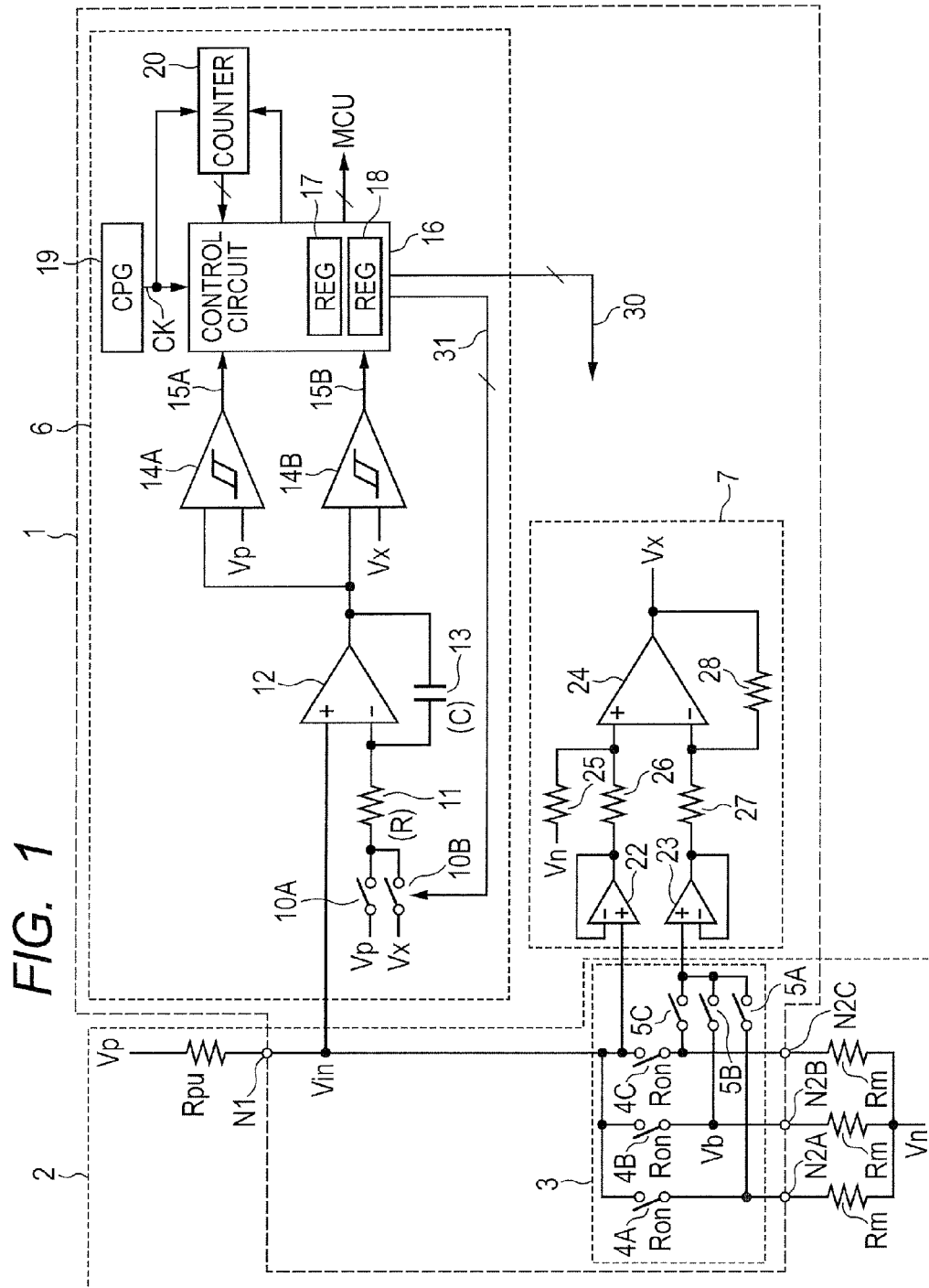


FIG. 2

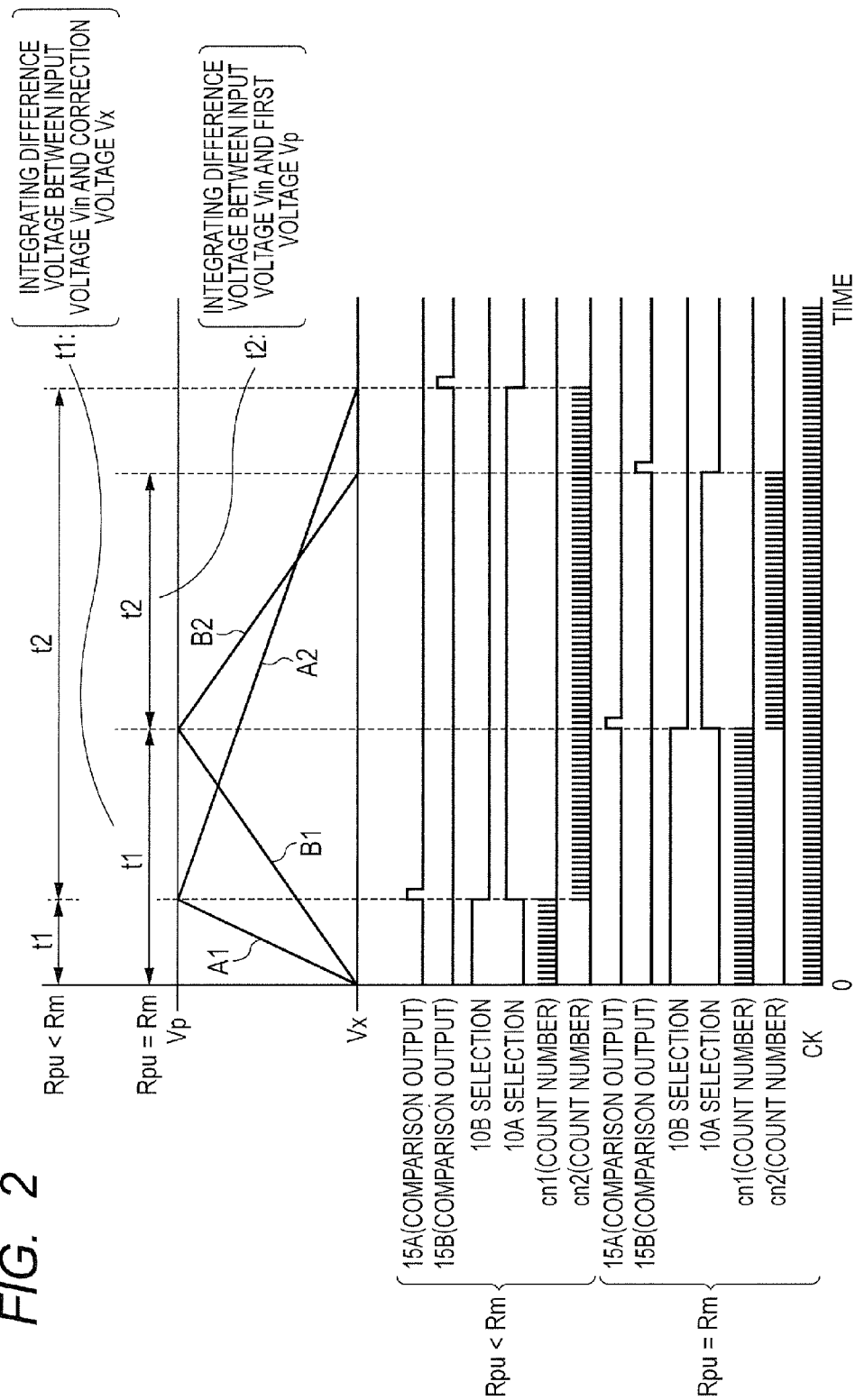


FIG. 3

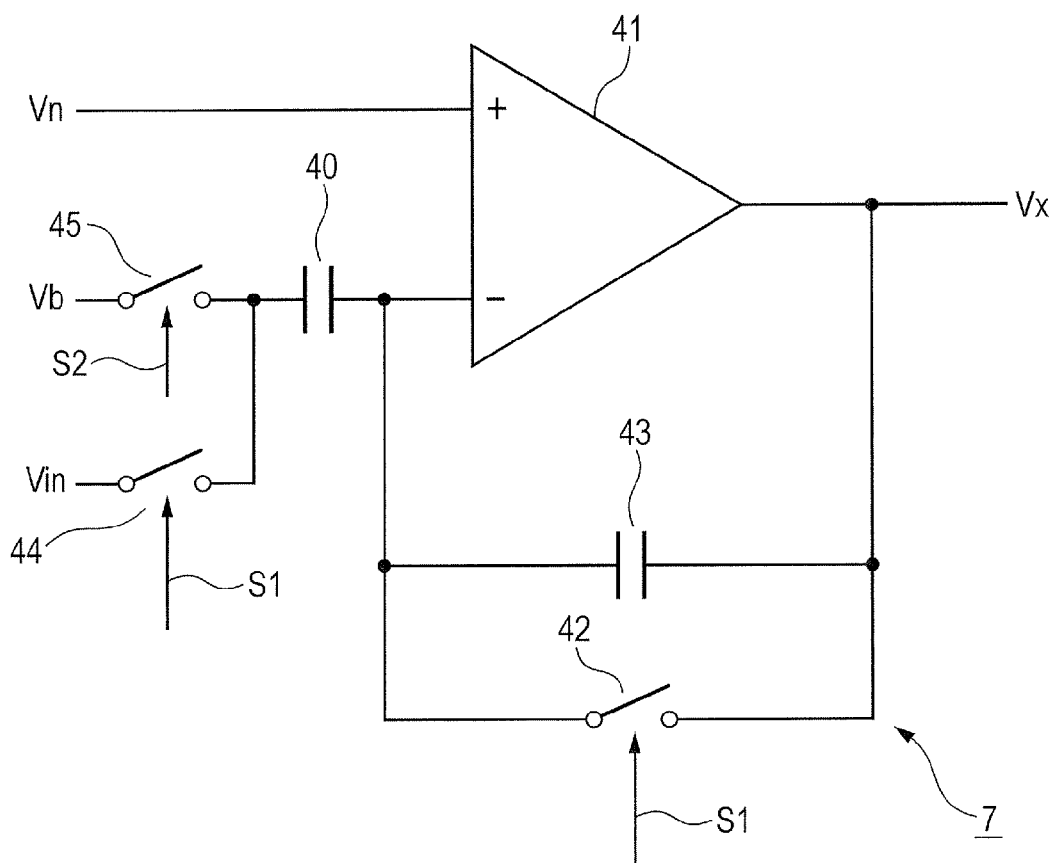
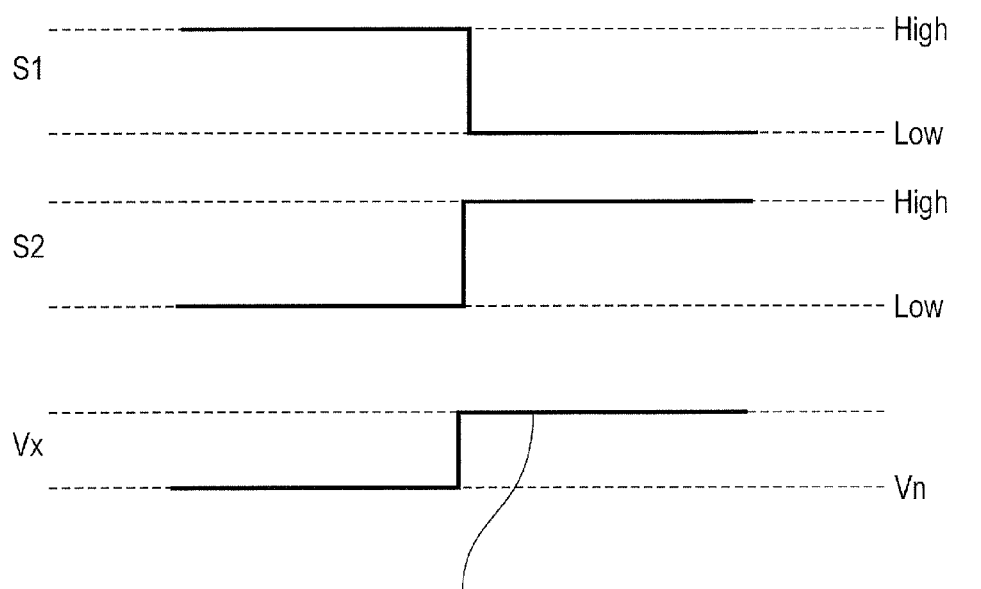


FIG. 4



$$V_x = V_n + (V_{in} - V_b)$$

$$= \frac{R_{on}}{R_{pu} + R_m + R_{on}} \cdot V_p + \frac{R_{pu} + R_m}{R_{pu} + R_m + R_{on}} \cdot V_n$$

FIG. 5

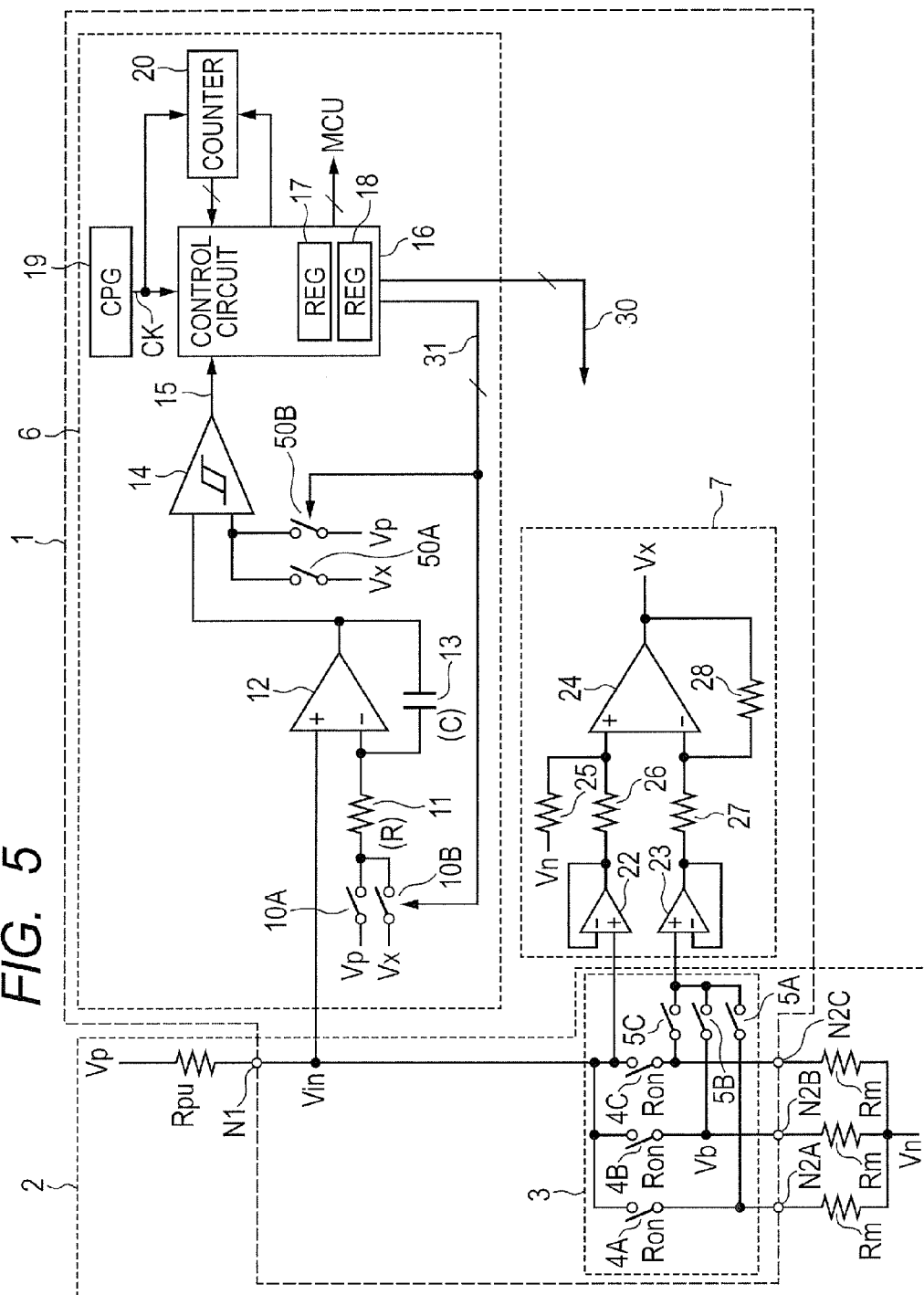


FIG. 6

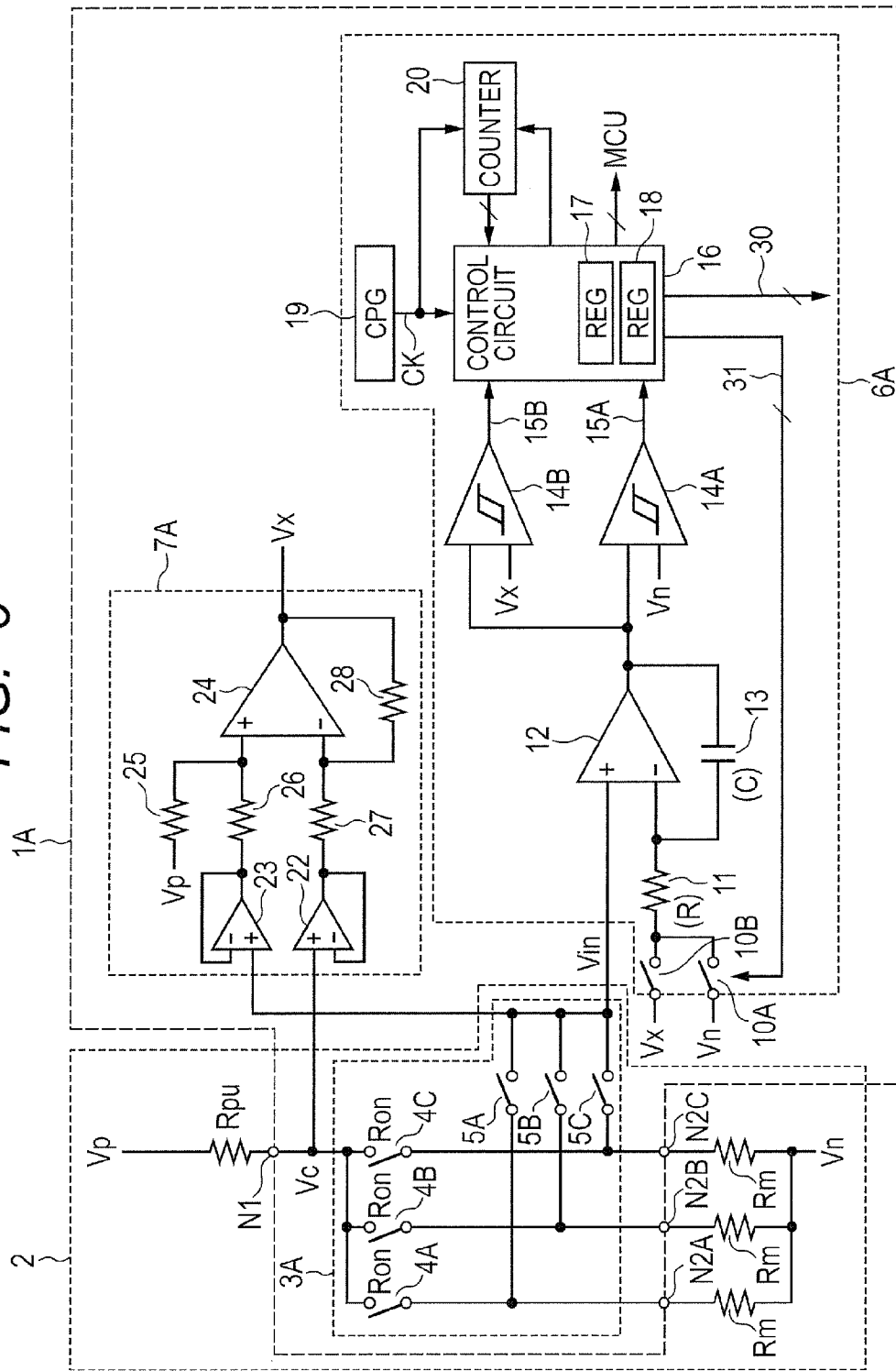


FIG. 7

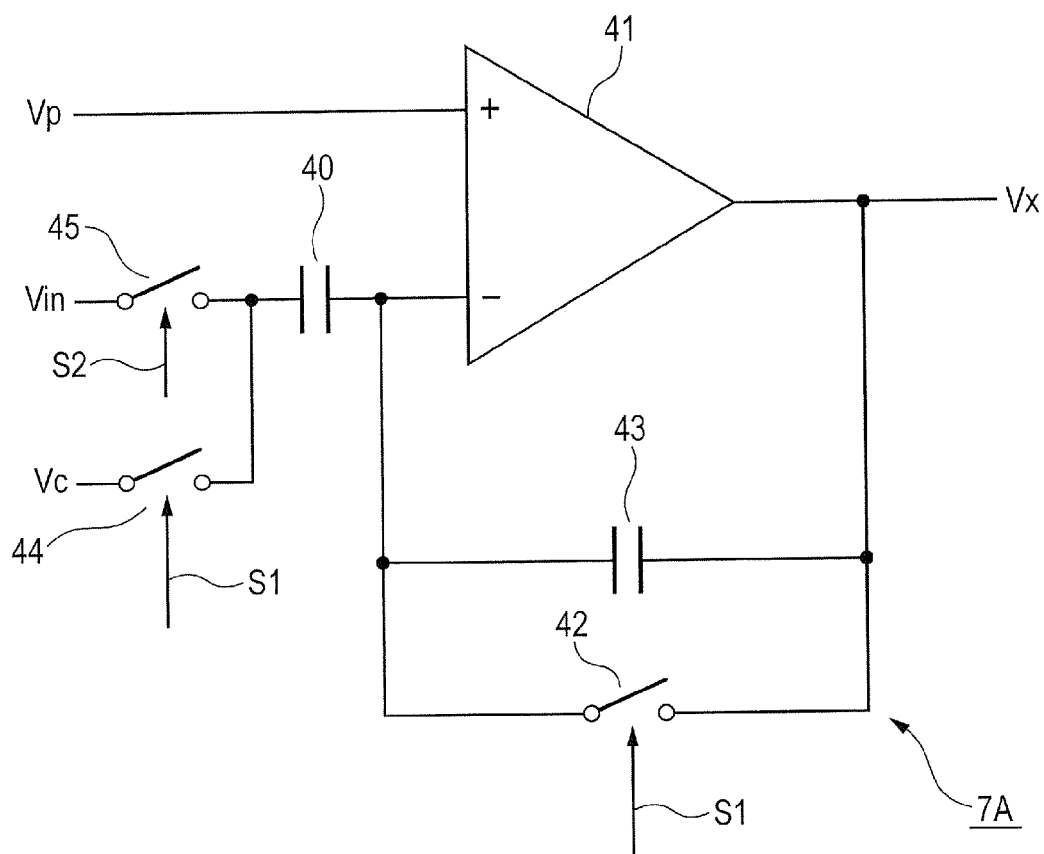




FIG. 8

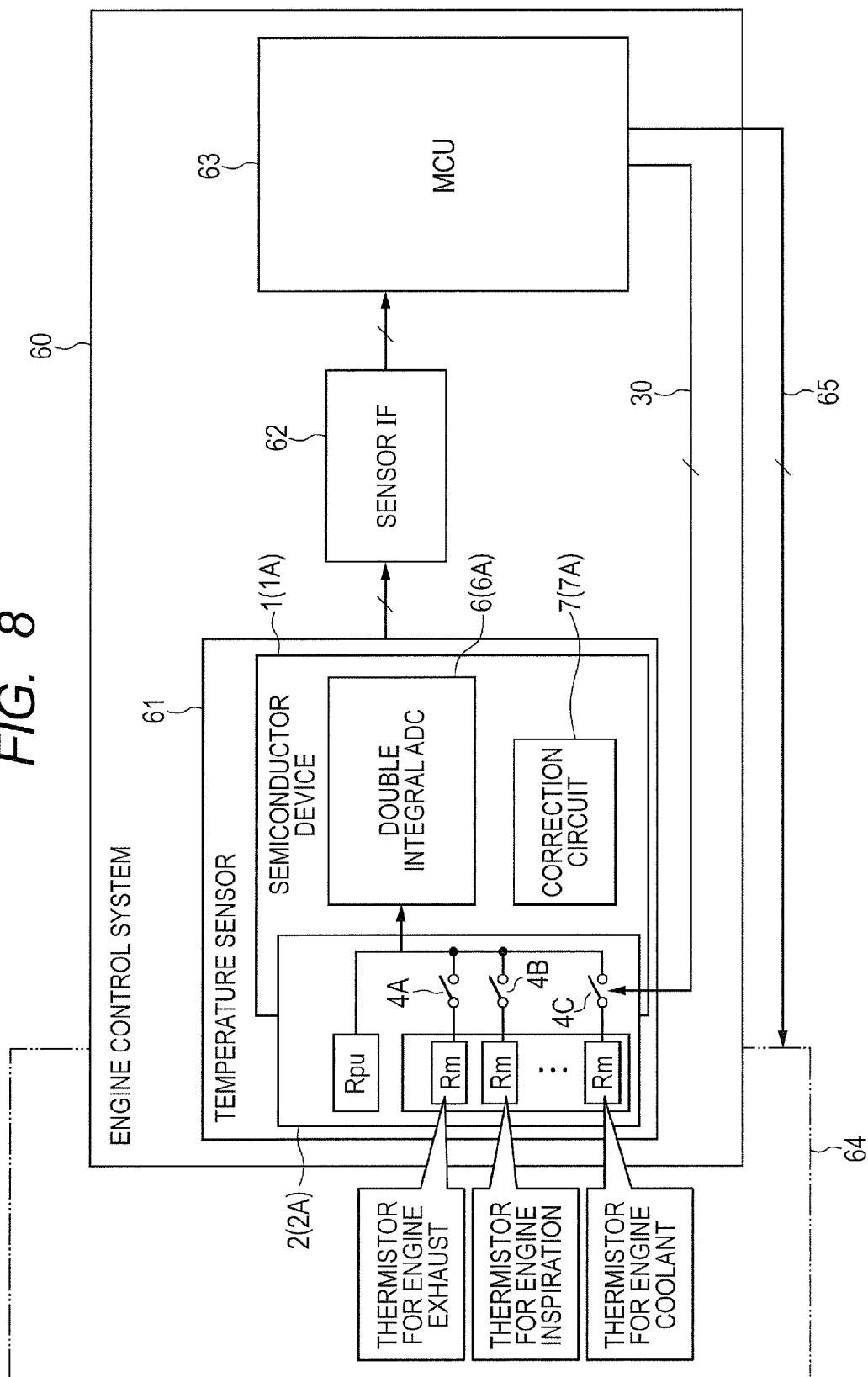
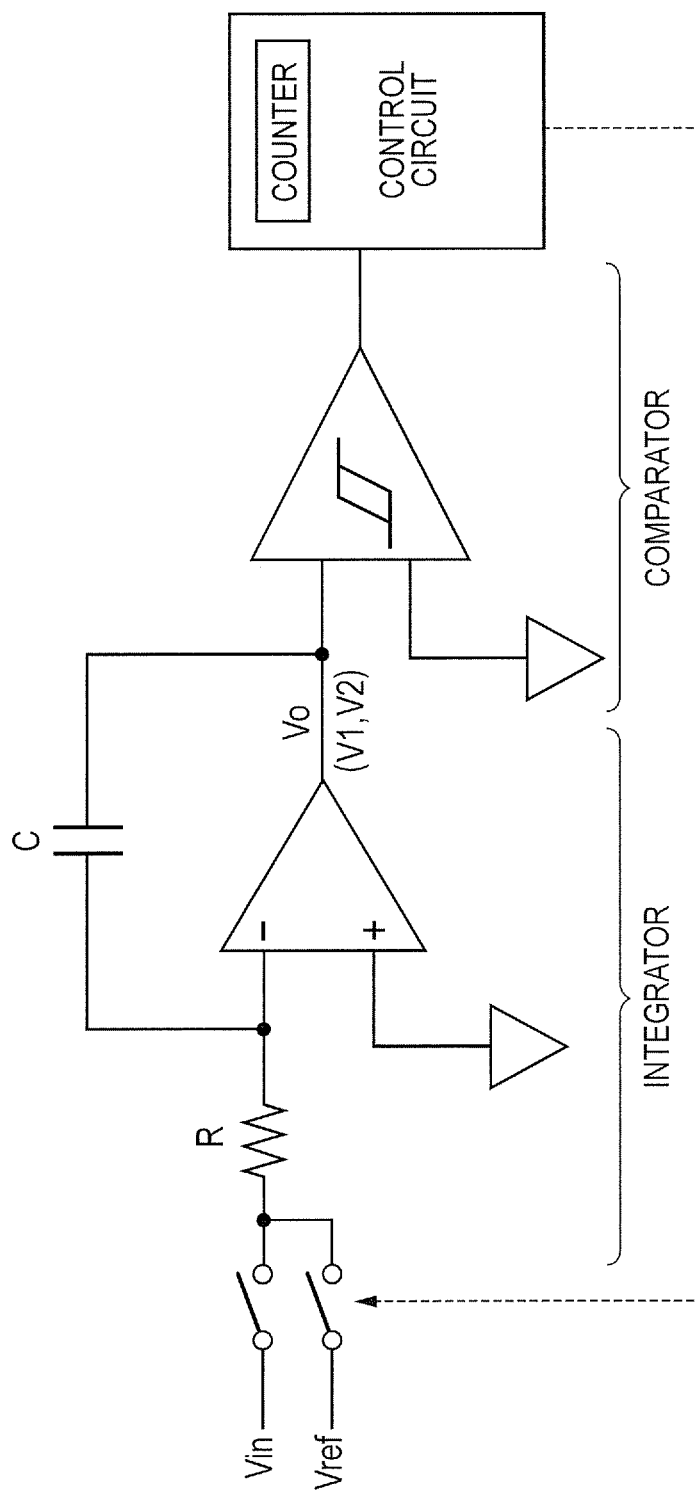


FIG. 9



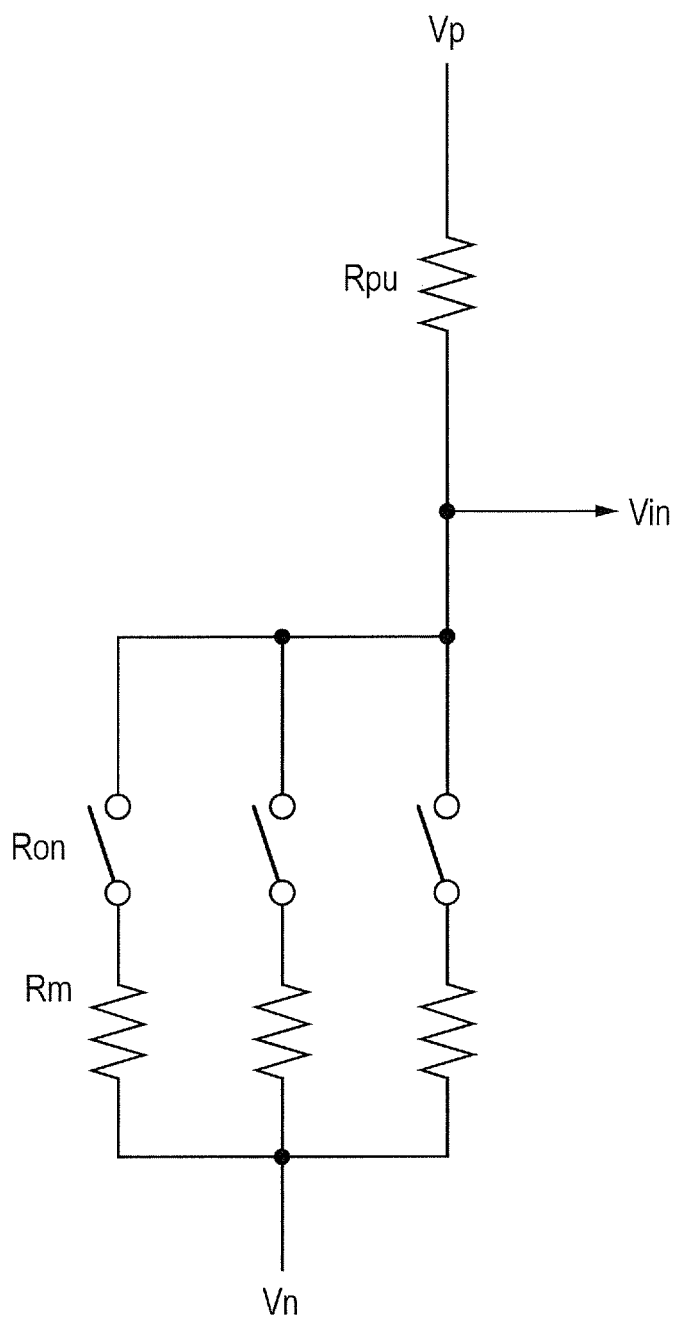
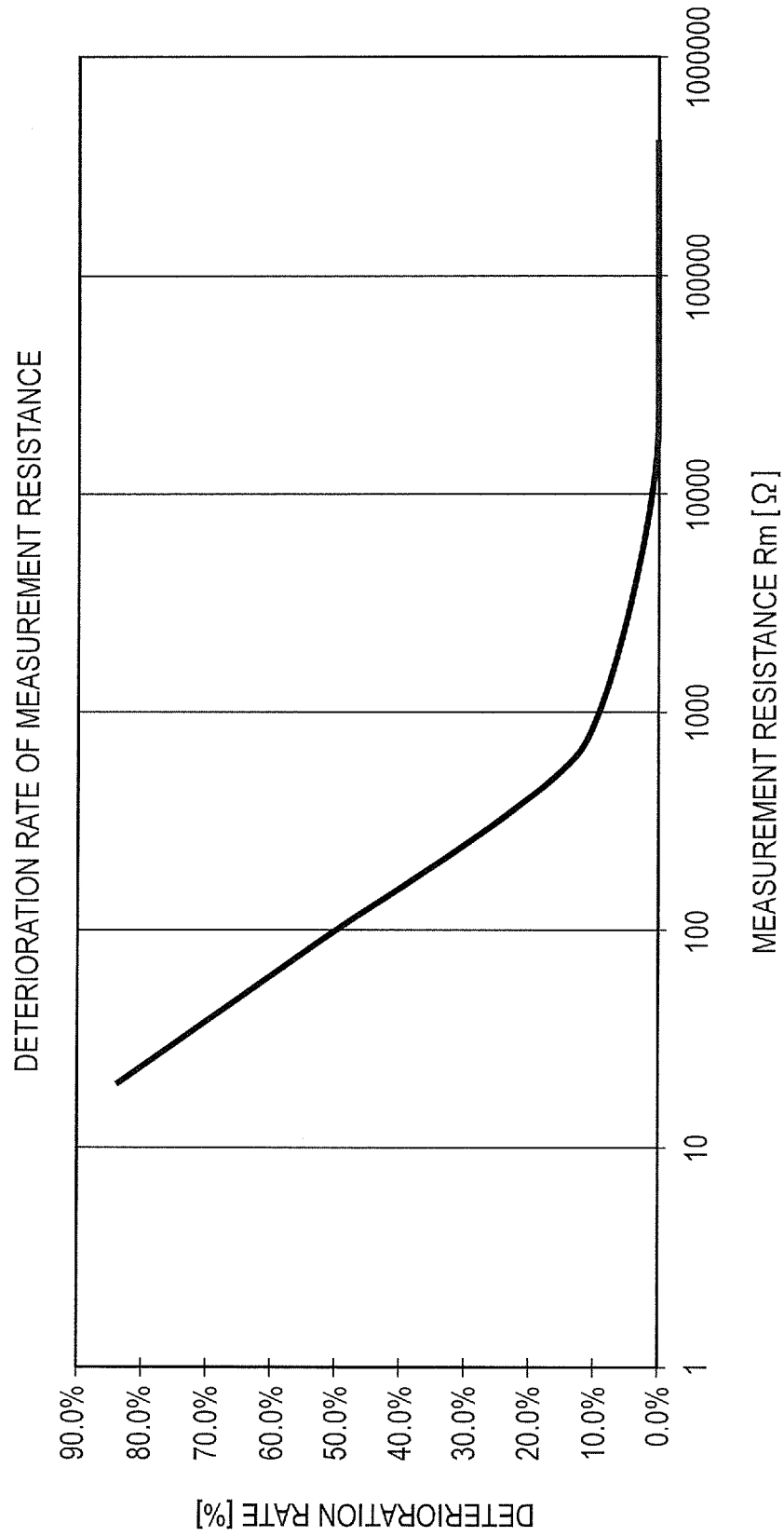
*FIG. 10*

FIG. 11



1

**SEMICONDUCTOR DEVICE AND  
ELECTRONIC CONTROL DEVICE****CROSS-REFERENCE TO RELATED  
APPLICATIONS**

The disclosure of Japanese Patent Application No. 2013-217508 filed on Oct. 18, 2013 including the specification, drawings and abstract is incorporated herein by reference in its entirety.

**BACKGROUND**

The present invention relates to a semiconductor device having a double integral analog-digital conversion circuit, and furthermore, an electronic control device using the analog-digital conversion circuit, and relates to a technology effective when being applied to an electronic control device for controlling an apparatus such as a power train while monitoring a resistance in a measurement sensor, for example, in an in-vehicle system.

In order to monitor a resistance of a measurement sensor, the double integral analog-digital conversion circuit can be used from its feature of being capable of high precision conversion in a simple circuit. As a representative of the double integral analog-digital conversion circuit, for example, as described in Japanese Unexamined Patent Application Publication No. 2012-39273, there is a circuit for finding a digital output by integrating an input voltage and a reference voltage whose polarity is opposite to the value two times in succession with a Miller integrating circuit. For example, an input voltage  $V_{in}$  can be found by counting a time elapsed when a voltage of an integrator varies from an output voltage  $V_0$  obtained by integrating the input voltage  $V_{in}$  for a specified time to a voltage of 0 V obtained by integrating the reference voltage  $V_{ref}$ . When assuming the double integral analog-digital conversion circuit of FIG. 9, a conversion operation is performed by integrating the analog input voltage  $V_{in}$  with an integrator with and subsequently integrating the reference voltage  $V_{ref}$  with the integrator again.  $V_1$  during a period when the analog input voltage  $V_{in}$  is integrated by the Miller integrating circuit becomes as shown by Formula 1. Incidentally, parameters in the following Formula 1 to Formula 3 are as follows.  $V_1$ : output voltage  $V_0$  of the integrator at the time of integrating the input voltage  $V_{in}$ ;  $V_2$ : output voltage  $V_0$  of the integrator at the time of integrating the reference voltage  $V_{ref}$ ;  $t_1$ : the specified time;  $N_2$ : pulse count at time  $t_1$ ;  $t_2$ : integral time of the reference voltage  $V_{ref}$ ; and  $n$ : pulse count at time  $t_2$  (digital output).

[Formula 1]

$$V_1 = -\frac{V_{in}}{RC}t_1 = \frac{V_{in}}{RC}NT \quad (1)$$

$V_2$  during a period when the reference voltage  $V_{ref}$  is integrated by the integrator becomes as shown by Formula 2.

[Formula 2]

$$V_2 = V_1 - \frac{1}{RC}(-V_{ref})t_2 = V_1 - \frac{1}{RC}(-V_{ref})nT \quad (2)$$

2

In Formula 2, it shall be integrated until  $V_2$  becomes  $V_2=0$  and a relationship of Formula 3 is obtained by substituting Formula 1 into this.

[Formula 3]

$$n = \frac{V_{in}}{V_{ref}} \cdot N \quad (3)$$

As is clear from Formula 3, the input voltage  $V_{in}$  is converted into the pulse count (digital output) of  $n$ .

For example, when intending to monitor a resistance of a thermistor of a temperature sensor, a reference resistance can be coupled in series to the thermistor serving as the measurement resistance and its divided voltage can be used as the input voltage. If the reference resistance  $R_{pu}$  and the measurement resistance  $R_m$  are coupled in series between the reference voltages  $V_p$ ,  $V_n$  and a voltage of their binding node is used as the input voltage  $V_{in}$ , the measurement resistance  $R_m$  can be found by Formula 4.

[Formula 4]

$$R_m = \frac{V_n - V_{in}}{V_{in} - V_p} \cdot R_{pu} \quad (4)$$

**SUMMARY**

In order to measure multiple measurement resistances by achieving commonality of the double integral analog-digital conversion circuit among them, for example, as illustrated in FIG. 10, multiple measurement resistances can be monitored by providing multiple measurement resistances  $R_m$  to a common reference resistance  $R_{pu}$  and coupling the measurement resistance selected by a multiplexer to the reference resistance in series.

However, the switching device of the multiplexer has not a little on-resistance  $R_{on}$ . By such an on-resistance being added to the measurement resistance  $R_m$ , an input voltage  $V_{in}$  that is different from assumption will be inputted into the double integral analog-digital conversion circuit, which will cause a problem that measurement accuracy of the measurement resistance  $R_m$  becomes deteriorated. Since the above-mentioned on-resistance has a temperature dependence and is affected by manufacture variation, it is not easy to grasp the value correctly.

A formula for finding the measurement resistance  $R_m$  from a configuration of FIG. 10 that takes the on-resistance into consideration becomes Formula 5.

[Formula 5]

$$R_m = \frac{V_n - V_{in}}{V_{in} - V_p} \cdot R_{pu} - R_{on} \quad (5)$$

As is clear from Formula 5, even if the input voltage can be found by the double integral analog-digital conversion circuit, it is impossible to find a correct resistance value of the measurement resistance  $R_m$  because a value of the on-resistance  $R_{on}$  of the switch of Formula 5 is unknown. If the measurement resistance  $R_m$  is measured without taking the on-resistance  $R_{on}$  of the switch into consideration, no con-

sideration of the on-resistance of the switch, as it is, will lead to deterioration of the measurement accuracy. When paying attention to a configuration of the double integral analog-digital conversion circuit of FIG. 9, unconformity that the on-resistance of the switch in the input circuit of FIG. 10 affects only charging of the input voltage  $V_{in}$  in double integral and does not affect charging of the reference voltage lowers detection accuracy of the measurement resistance.

The above-mentioned and other problems and new features will become clear from the following description and the accompanying drawings of this specification.

Explaining briefly a representative embodiment among embodiments that are disclosed in this application, it will be as described below.

That is, selector switches are provided between a first node coupled to a first voltage through the reference resistance and multiple second nodes coupled to a second voltage through measurement resistances, and the second node to be coupled to the first node is selected by the selector switches. A correction circuit that generates a voltage obtained by adding the second voltage to a voltage between the second node selected by the selector switches and the first node as a correction voltage is provided. The double integral analog-digital conversion circuit finds a first integral time elapsed when a difference voltage of the correction voltage with respect to a voltage of the first node is integrated to the first voltage and a second integral time elapsed when a difference voltage of the first voltage with respect to the voltage of the first node is integrated to the correction voltage.

Explaining briefly an effect that can be obtained by a representative embodiment among embodiments disclosed in this application, it will be as follows.

That is, since an influence of an on-resistance of the selector switch comes to be consistent between the first integral and the second integral of the double integral, it is possible to suppress the detection accuracy of the measurement resistance from decreasing caused by the on-resistance of the selector switch.

### BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram of a semiconductor device having a double integral analog-digital conversion circuit;

FIG. 2 is a timing chart for illustrating operation timings of a first integral operation and a second integral operation;

FIG. 3 is a block diagram showing another example of a correction circuit;

FIG. 4 is a timing chart for illustrating an operation timing of the correction circuit of FIG. 3;

FIG. 5 is a block diagram for illustrating the double integral analog-digital conversion circuit that adopts another example of a comparator circuit;

FIG. 6 is a block diagram for showing a second example of the semiconductor device having the double integral analog-digital conversion circuit;

FIG. 7 is a block diagram for showing another example of the correction circuit;

FIG. 8 is a block diagram for illustrating an engine control system mounted on an automobile as one example of an electronic control device;

FIG. 9 is an explanatory diagram of the double integral analog-digital conversion circuit having been provided in the related art;

FIG. 10 is a circuit diagram for illustrating an input circuit that forms an input voltage of the double integral analog-

digital conversion circuit by coupling the measurement resistance selected by a multiplexer to a reference resistance in series; and

FIG. 11 is an explanatory diagram for showing that in the case where the resistance value of the measurement resistance is small, the measurement resistance is susceptible to be affected by an on-resistance of a selector switch.

### DETAILED DESCRIPTION

#### 1. Outline of Embodiment

First, an outline about embodiments disclosed in this application will be explained. In the explanation of the outline about the embodiments, any reference numeral in the drawing that is referred to with a parenthesis attached merely illustrates what is included in a concept of a component.

[1] <<FIG. 1, Semiconductor Device>>

A semiconductor device (1) has: a first node (N1) coupled to a first voltage ( $V_p$ ) through a reference resistance ( $R_{pu}$ ); multiple second nodes (N2A, N2B, and N2C) coupled to a second voltage ( $V_n$ ) through measurement resistances ( $R_m$ ); multiple selector switches (4A, 4B, and 4C) for selecting the second node to be coupled to the first node; a correction circuit (7) that generates a voltage obtained by adding the second voltage to the voltage between the second node selected by the selector switches and the first node as a correction voltage ( $V_x$ ); and a double integral analog-digital conversion circuit (6) that finds a first integral time ( $t_1$ ) elapsed when a difference voltage of the correction voltage with respect to the voltage of the first node is integrated to the first voltage and a second integral time ( $t_2$ ) elapsed when a difference voltage of the first voltage with respect to the voltage of the first node is integrated to the correction voltage.

According to this, a voltage ( $V_{in}$ ) of the first node is a sum of the second voltage ( $V_n$ ), a drop voltage ( $IR_m$ ) by the measurement resistance ( $R_m$ ), and a drop voltage ( $IR_{on}$ ) by the selector switch. The correction voltage ( $V_x$ ) is a sum of the second voltage ( $V_n$ ) and the drop voltage ( $IR_{on}$ ) by the selector switch. Therefore, an integral time of a first integral operation elapsed when a difference voltage ( $V_{in}-V_x=IR_m$ ) of the correction voltage ( $V_x$ ) to the voltage of the first node is integrated to the first voltage does not include a component of an on-resistance of the selector switch. Moreover, since the first voltage is a sum of the second voltage ( $V_n$ ), the drop voltage ( $IR_m$ ) by the measurement resistance ( $R_m$ ), the drop voltage ( $IR_{on}$ ) by the selector switch, and the drop voltage ( $IR_{pu}$ ) by the reference resistance ( $R_{pu}$ ), the integral time of a second integral operation elapsed when a difference voltage ( $V_{in}-V_p=-IR_{pu}$ ) of the first voltage to the voltage of the first node is integrated to the correction voltage does not include the component of the on-resistance of the selector switch similarly. Therefore, since an influence of the on-resistance of the selector switch comes to be consistent between the first integral and the second integral of double integral, it is possible to suppress detection accuracy of the measurement resistance from decreasing caused by the on-resistance of the selector switch, which enables the resistance value of the measurement resistance to be measured with high precision.

[2] <<Integrating Circuit, Detection Circuit, and Control Circuit>>

In the clause 1, the double integral analog-digital conversion circuit has: an integrating circuit (12) that performs the first integral operation of integrating the difference voltage of the correction voltage with respect to the first node and the second integral operation of integrating the difference voltage of the first voltage with respect to the voltage of the first node;

5

detection circuits (14A, 14B, 14) that generate a first detection signal (15A) when an integral output of the integrating circuit reaches the first voltage in the first integral operation and generate a second detection signal (15B) when an integral output of the integrating circuit reaches the correction voltage in the second integral operation; a counter (20) for counting a clock signal (CK); and a control circuit (16) that acquires a first count value (N) by the counter from when the first integral operation is started by the integrating circuit until the first detection signal is generated and a second count value (n) by the counter from when the second integral operation is started thereby until the second detection signal is generated.

According to this, the double integral analog-digital conversion circuit can be comparatively easily formed.

[3] <<Miller Integrating Circuit>>

In the clause 2, the integrating circuit is a Miller integrating circuit (12) that receives the voltage of the first node at its noninverting input terminal and receives selectively the first voltage or the correction voltage at its inverting input terminal.

According to this, the integrating circuit can be comparatively easily formed using an operational amplifier.

[4] <<Correction Circuit by Buffer Amplifier and Differential Amplifier>>

In the clause 1, the correction circuit has: a first buffer amplifier (22) for receiving the voltage of the first node; a second buffer amplifier (23) for receiving a voltage of the second node selected by the selector switches; and a differential amplifier (24) that forms a voltage obtained by adding the second voltage to a difference voltage of the output of the second buffer amplifier with respect to the output of the first buffer amplifier as the correction voltage.

According to this, the correction circuit can be comparatively easily formed using an operational amplifier.

[5] <<Correction Circuit by Switched Capacitor Circuit>>

In the clause 1, the correction circuit has: an operational amplifier (41) that receives the second voltage at its noninverting input terminal and to which one capacitance electrode of the input capacitance is bound at its inverting input terminal; a first switch (42) that makes feedback coupling of an output terminal of the operational amplifier to the inverting input terminal; a feedback capacitance (43) coupled to the first switch in parallel; a second switch (44) that is switch-controlled in phase with the first switch and applies the voltage of the first node to the other capacitance electrode of the input capacitance in the ON state; and a third switch (45) that is switch-controlled in reverse phase with the first switch and applies the voltage of the second nodes to the other capacitance electrode of the input capacitance in the ON state.

According to this, the number of operational amplifiers can be reduced compared with the correction circuit of the clause 4.

[6] <<First Node and Second Nodes are External Terminals>>

In the clause 1, the first node and the second nodes are external terminals.

According to this, necessity for an input into the double integral circuit is reduced to simply a matter of preparing the reference resistance and the measurement resistance as external circuit elements of the semiconductor device.

[7] <<FIG. 6, Semiconductor Device>>

A semiconductor device (1A) has: a first node (N1) coupled to a first voltage (Vp) through the reference resistance (Rpu); multiple second nodes (N2A, N2B, and N2C) coupled to the second voltage (Vn) through measurement resistances (Rm); multiple selector switches (4A, 4B, and 4C) for selecting the second node to be coupled to the first node;

6

a correction circuit (7A) that generates a voltage obtained by subtracting the voltage between the second node selected by the selector switches and the first node from the first voltage as the correction voltage (Vx); and a double integral analog-digital conversion circuit (6A) that finds the first integral time (t1) elapsed when the difference voltage of the correction voltage with respect to the voltage of the second nodes is integrated to the second voltage and the second integral time (t2) elapsed when a difference voltage of the second voltage with respect to the voltage of the second nodes is integrated to the correction voltage.

According to this, the voltage (Vin) of the second nodes is a sum ( $V_{in} = V_n + IR_m$ ) of the second voltage (Vn) and the drop voltage (IRm) by the measurement resistance (Rm). The correction voltage (Vx) is a voltage ( $V_x = V_p - IR_{on}$ ) obtained by subtracting the drop voltage (IRon) by the selector switch from the first voltage (Vp). Since  $V_p = V_n + IR_m + IR_{on} + IR_{up}$  holds here, the integral time of the first integral operation elapsed when the difference voltage ( $V_{in} - V_x = -IR_{pu}$ ) of the correction voltage (Vx) to the voltage (Vin) of the second nodes is integrated to the first voltage does not include the component of the on-resistance of the selector switch. Moreover, the integral time of the second integral operation when the difference voltage ( $V_{in} - V_n = IR_m$ ) of the second voltage to the voltage of the second nodes is integrated to the correction voltage does not include the component of the on-resistance of the selector switch similarly. Therefore, since the influence of the on-resistance of the selector switch comes to be consistent between the first integral and the second integral of the double integral, it is possible to suppress the detection accuracy of the measurement resistance from decreasing caused by the on-resistance of the selector switch, which enables the resistance value of the measurement resistance to be measured with high precision.

[8] <<Integrating Circuit, Detection Circuit, and Control Circuit>>

In the clause 7, the double integral analog-digital conversion circuit has: the integrating circuit (12) that performs the first integral operation of integrating the difference voltage of the correction voltage with respect to the voltage of the second nodes and the second integral operation of integrating the difference voltage of the second voltage with respect to the voltage of the second nodes; the detection circuits (14A, 14B) that generate the first detection signal (15A) when the integral output of the integrating circuit reaches the second voltage in the first integral operation and generates the second detection signal (15B) when the output of the integrating circuit reaches the correction voltage in the second integral operation; the counter (20) for counting the clock signal (CK); and the control circuit (16) that acquires the first count value (N) by the counter from when the first integral operation is started by the integrating circuit until the first detection signal is generated and the second count value (n) by the counter from when the second integral operation is started thereby until the second detection signal is generated.

According to this, the double integral analog-digital conversion circuit can be comparatively easily formed.

[9] <<Miller Integrating Circuit>>

In the clause 8, the integrating circuit is the Miller integrating circuit (12) that receives the voltage of the second nodes at its noninverting input terminal and receives selectively the second voltage or the correction voltage at its inverting input terminal.

According to this, the integrating circuit can be comparatively easily formed using an operational amplifier.

[10] <<Correction Circuit by Buffer Amplifier and Differential Amplifier>>

In the clause 7, the correction circuit has: a first buffer amplifier (22) for receiving the voltage of the first node; a second buffer amplifier (23) for receiving the voltage of the second node selected by the selector switches; and a differential amplifier (24) that forms a voltage obtained by subtracting a difference voltage of the output of the second buffer amplifier with respect to the output of the first buffer amplifier from the first voltage as the correction voltage.

According to this, the correction circuit can be comparatively easily formed using an operational amplifier.

[11] <<Correction Circuit by Switched Capacitor Circuit>>

In the clause 7, the correction circuit includes: the operational amplifier (41) that receives the first voltage at its non-inverting input terminal and to which one capacitance electrode of the input capacitance is bound at its inverting input terminal; the first switch (42) that makes feedback coupling of the output terminal of the operational amplifier to the inverting input terminal; the feedback capacitance (43) that is coupled to the first switch in parallel; the second switch (44) that is switch-controlled in phase with the first switch and applies the voltage of the first node to the other capacitance electrode of the input capacitance in the ON state; and the third switch (45) that is switch-controlled in reverse phase with the first switch and applies the voltage of the second nodes to the other capacitance electrode of the input capacitance in the ON state.

According to this, the number of operational amplifiers can be reduced compared with the correction circuit of the clause 4.

[12] <<First Node and Second Nodes are External Terminals>>

In the clause 7, the first node and the second nodes are external terminals.

According to this, necessity for an input into the double integral circuit is reduced to simply a matter of preparing the reference resistance and the measurement resistance as external circuit elements of the semiconductor device.

[13] <<Electronic Control Device Adopting Configuration of FIG. 1>>

An electronic control device (60) has: multiple measurement resistances provided in a control object apparatus (63); the reference resistance; the first node coupled to the first voltage through the reference resistance; the multiple second nodes coupled to the second voltage through the measurement resistances; the multiple selector switches for selecting the second node to be coupled to the first node; a correction circuit (7) that generates a voltage obtained by adding the second voltage to the voltage between the second node selected by the selector switches and the first node as the correction voltage; the double integral analog-digital conversion circuit (6) that finds the first integral time elapsed when the difference voltage of the correction voltage with respect to the voltage of the first node is integrated to the first voltage and the second integral time elapsed when the difference voltage of the first voltage with respect to the voltage of the first node is integrated to the correction voltage; and a control part that is for inputting therein the first integral time and the second integral time, calculating a value obtained by multiplying a ratio of the first integral time to the second integral time by a resistance value of the reference resistance as the resistance value of the measurement resistance, and controlling the control object apparatus based on the calculation result.

According to this, like the clause 1, since the influence of the on-resistance of the selector switch comes to be consistent

between the first integral and the second integral of the double integral, it is possible to suppress the detection accuracy of the measurement resistance from decreasing caused by the on-resistance of the selector switch, which enables the resistance value of the measurement resistance to be measured with high precision. Therefore, reliability of the control for the control object apparatus can be increased.

[14] <<Thermistor>>

In the clause 13, the measurement resistance is a thermistor used for thermometry.

According to this, the reliability of the control for the control object apparatus based on a measurement result of temperature can be increased.

[15] <<Engine Control>>

In the clause 14, the control object apparatus is an automobile engine.

According to this, the reliability of the control for the automobile engine based on the measurement result of temperature can be increased.

[16] <<Photoconductive Cell>>

In the clause 13, the measurement resistance is a photoconductive cell used for photodetection.

According to this, the reliability of the control for the control object apparatus based on a measurement result of light can be increased.

[17] <<Gas Concentration Measurement>>

In the clause 13, the measurement resistance is a resistance element used for gas concentration measurement.

According to this, the reliability of the control for the control object apparatus based on the measurement result of gas concentration can be increased.

[18] <<Electronic Control Device Adopting Configuration of FIG. 6>>

The electronic control device (60) has: multiple measurement resistances provided in the control object apparatus (63); the reference resistance; the first node coupled to the first voltage through the reference resistance; the multiple second nodes coupled to the second voltage through the measurement resistances; the multiple selector switches for selecting the second node to be coupled to the first node; the correction circuit (7A) that generates a voltage obtained by subtracting the voltage between the second node selected by the selector switches and the first node from the first voltage as the correction voltage; the double integral analog-digital conversion circuit (6A) that finds the first integral time elapsed when the difference voltage of the correction voltage with respect to the voltage of the second nodes is integrated to the second voltage and the second integral time elapsed when the difference voltage of the second voltage with respect to the voltage of the second nodes is integrated to the correction voltage; and a control part for inputting therein the first integral time and the second integral time, calculating a value obtained by multiplying a ratio of the first integral time to the second integral time by the resistance value of the reference resistance as a resistance value of the measurement resistance, and controlling the control object apparatus based on the calculation result.

According to this, like the clause 7, since the influence of the on-resistance of the selector switch comes to be consistent between the first integral and the second integral of the double integral, it is possible to suppress the detection accuracy of the measurement resistance from decreasing caused by the on-resistance of the selector switch, which enables the resistance value of the measurement resistance to be measured with high



precision. Therefore, the reliability of the control for the control object apparatus can be increased.

## 2. Details of Embodiments

Embodiments will be explained further in detail.

<<First Embodiment of Semiconductor Device>>

FIG. 1 shows one example of a semiconductor device having a double integral analog-digital conversion circuit. Although the semiconductor device shown in the figure is especially not limited, it is formed over one semiconductor substrate such as of single crystal silicon with a known CMOS integrated circuit manufacturing technology.

A semiconductor device 1 shown in FIG. 1 forms, for example, a temperature sensor with the reference resistance  $R_{pu}$  and multiple (e.g., three) measurement resistances  $R_m$  attached externally. It is not required that the measurement resistances  $R_m$  shall be the same.

Since a part of an input circuit 2 is comprised of the semiconductor device 1 through the above-mentioned reference resistance  $R_{pu}$  and multiple measurement resistances  $R_m$ , the semiconductor device 1 has a first node N1 coupled to a first voltage  $V_p$  through the reference resistance  $R_{pu}$ , the multiple second nodes N2A, N2B, and N2C coupled to a second voltage  $V_n$  through the respective measurement resistances  $R_m$ , and the multiple selector switches 4A, 4B, and 4C for selecting the second node N2A, N2B, or N2C to be coupled to the first node. An on-resistance of the selector switches 4A, 4B, and 4C is designated as  $R_{on}$ . A current path extending from the first voltage  $V_p$  to the second voltage  $V_n$  is formed by any one of the selector switches 4A, 4B, and 4C being turned on, and a voltage of the first node N1 and a voltage of the second nodes N2i (i=A, B, and C) that are formed by resistance voltage division are shown in the figure as  $V_{in}$  and  $V_b$ , respectively. Selective switches 5A, 5B, and 5C for inputting a voltage of the selected selector switch 4A, 4B, or 4C on the side of the second node N2A, N2B, or N2C in response to an on-operation of the selector switch 4A, 4B, or 4C are arranged. A detection channel switching circuit 3 is comprised of the selector switches 4A, 4B, and 4C and the selective switches 5A, 5B, and 5C. Although being especially not limited, switch control of the detection channel switching circuit 3 is performed by a control signal 30 outputted from a control circuit 16, or is performed by another logic circuit whose illustration is omitted. Incidentally, the first voltage  $V_p$  and the second voltage  $V_n$  may be voltages generated by a power supply circuit of the semiconductor device 1, or may be voltages given from the outside of the semiconductor device 1.

The semiconductor device 1 has a double integral analog-digital conversion circuit (also described as double integral ADC) 6 and a correction circuit 7.

The correction circuit 7 generates a voltage obtained by adding the second voltage  $V_n$  to a voltage between the second node N2A, N2B, or N2C selected by selector switches 4A, 4B, and 4C and the first node N1 as a correction voltage  $V_x$ . For example, in FIG. 1, the correction circuit 7 has: a first buffer amplifier 22 that receives a voltage  $V_{in}$  of the first node N1; a second buffer amplifier 23 that receives a voltage  $V_b$  of the second node N2A, N2B, or N2C selected by the selector switches 4A, 4B, and 4C through the selective switch 5A, 5B, or 5C; and a differential amplifier 24 that forms a voltage obtained by adding the second voltage  $V_n$  to a difference voltage of an output of the second buffer amplifier 23 with respect to an output of the first buffer amplifier 22 as the correction voltage  $V_x$ . Resistances 25, 26, 27, and 28 are for gain adjustment.

A double integral ADC 6 finds a first integral time  $t_1$  elapsed when a difference voltage of the correction voltage  $V_x$  with respect to the voltage  $V_{in}$  of the first node N1 is integrated to the first voltage  $V_p$  and a second integral time  $t_2$  elapsed when a difference voltage of the first voltage  $V_p$  with respect to the voltage  $V_{in}$  of the first node N1 is integrated to the correction voltage  $V_x$ . Further in detail, the double integral ADC 6 has, in its first stage, a Miller integrating circuit 12 that receives the voltage  $V_{in}$  of the first node N1 at its noninverting input terminal (+) and receives the first voltage  $V_p$  or the correction voltage  $V_x$  selected by switches 10A, 10B at its inverting input terminal (-). 13 is an integral capacity (C) and 11 is an integral resistor (R). Selection of the switches 10A, 10B is controlled by a control signal 31 outputted from the control circuit 16. The Miller integrating circuit 12 performs the first integral operation of integrating the difference voltage of the correction voltage  $V_x$  with respect to the voltage  $V_{in}$  of the first node N1 and the second integral operation of integrating the difference voltage of the first voltage  $V_p$  with respect to the voltage  $V_{in}$  of the first node N1. A hysteresis comparator 14A that generates a detection pulse (the first detection signal) 15A when an integral output of the Miller integrating circuit 12 reaches the first voltage  $V_p$  in the first integral operation and a hysteresis comparator 14B that generates a detection pulse (the second detection signal) 15B when the output of the Miller integrating circuit 12 reaches the correction voltage  $V_x$  in the second integral operation are arranged as comparator circuits.

The first detection signal 15A and the second detection signal 15B are supplied to the control circuit 16. The control circuit 16 operates by using a clock signal CK outputted from a clock generation circuit (CPG) 19 as a reference clock, and performs control of a counter 20 for counting the clock signal CK, selective control of the selective switches 10A, 10B, etc. The control circuit 16 controls operations that accumulates in a register 17 a first count value N counted by the counter 20 in a period spanning from making the integrating circuit 12 start the first integral operation by selecting the correction voltage  $V_x$  with the selective switch 10B until a first detection signal 14A is generated, and further accumulates in a register 18 a second count value n counted by the counter 20 in a period spanning from making the integrating circuit 12 start the second integral operation by selecting the first voltage  $V_p$  with the selective switch 10A until a second detection signal 14B is generated.

According to a configuration of FIG. 1, when one of the selector switches 4A, 4B, and 4C is selected, a current flowing into the second voltage  $V_n$  from the first voltage  $V_p$  is designated as I. At this time, the voltage  $V_{in}$  of the first node N1 is a sum ( $V_{in}=V_n+I R_m+I R_{on}$ ) of the second voltage  $V_n$ , a drop voltage  $I R_m$  by the measurement resistance  $R_m$ , and a drop voltage  $I R_{on}$  by the on-resistance of the selector switch. Moreover, the correction voltage  $V_x$  is a sum ( $V_x=V_n+I R_{on}$ ) of the second voltage  $V_n$  and the drop voltage  $I R_{on}$  by the selector switch. Therefore, an integral time  $t_1$  of the first integral operation elapsed when the difference voltage ( $V_{in}-V_x=I R_m$ ) of the correction voltage  $V_x$  to the voltage  $V_{in}$  of the first node N1 is integrated to the first voltage  $V_p$  does not include a component of an on-resistance  $R_{on}$  of the selector switches 4A, 4B, and 4C. Moreover, since the first voltage  $V_p$  is a sum ( $V_p=V_n+I R_m+I R_{on}+I R_{pu}$ ) of the second voltage  $V_n$ , the drop voltage  $I R_m$  by the measurement resistance  $R_m$ , the drop voltage  $I R_{on}$  by the selector switch, and the drop voltage  $I R_{pu}$  by the reference resistance  $R_{pu}$ , the integral time  $t_2$  of the second integral operation when the difference voltage ( $V_{in}-V_p=-I R_{pu}$ ) of the first voltage  $V_p$  to the voltage  $V_{in}$  of the first node N1 is integrated to the correction voltage  $V_x$

## 11

does not include the component of the on-resistance  $R_{on}$  of the selector switches 4A, 4B, and 4C.

FIG. 2 illustrates a timing chart of the first integral operation and the second integral operation. Waveforms A1, A2 of FIG. 2 show an integral waveform of the first integral operation and an integral waveform of the second integral operation, respectively, performed by the Miller integrating circuit 12 in the case of  $R_{pu} < R_m$ . Waveforms B1, B2 of FIG. 2 show an integral waveform of the first integral operation and an integral waveform of the second integral operation, respectively, performed by the Miller integrating circuit 12 in the case of  $R_{pu} = R_m$ . Since the component of the on-resistance  $R_{on}$  of the selector switches 4A, 4B, and 4C is included in neither the waveform of the first integral operation nor the waveform of the second integral operation, as described above,  $t_1 = t_2$  holds as shown in the integral waveforms B1, B2 in the case of  $R_{pu} = R_m$ .

As is clear from the explanation described above, the voltage drop by the on-resistance  $R_{on}$  of the selector switches 4A, 4B, and 4C affect neither the first integral operation nor the second integral operation performed by the Miller integrating circuit 12.

Next, how to acquire a value of the measurement resistance  $R_m$  by using count values  $cn_1$ ,  $cn_2$  that are made to correspond to  $t_1$ ,  $t_2$  for integral operation times obtained by the first integral operation and the second integral operation, respectively, without being affected by the voltage drop by the on-resistance  $R_{on}$  of the selector switches 4A, 4B, and 4C will be explained using mathematical expressions.

A charging operation of the waveform A1 of FIG. 2 can be expressed by Formula 6 and a charging operation of the waveform A2 of FIG. 2 can be expressed by Formula 7.

[Formula 6]

$$V_p - V_x = \frac{V_{in} - V_x}{R_c} t_1 \quad (6)$$

[Formula 7]

$$V_x - V_p = \frac{V_{in} - V_p}{RC} t_2 \quad (7)$$

If  $t_1$  and  $t_2$  are set to  $N$  and  $n$ , respectively, Formula 8 will be obtained from Formula 6 and Formula 7.

[Formula 8]

$$n = \frac{V_{in} - V_x}{V_p - V_{in}} \cdot N \quad (8)$$

Meanings of parameters in Formulae 6 to 8 are as follows.  $n$ : digital output (a count number in the period  $t_2$ ),  $N$ : count number in the period  $t_1$ ,  $V_{in}$ : voltage of the first node (an input voltage),  $V_x$ : output voltage of the correction circuit, and  $V_p$ : first voltage.

Here, the input voltage  $V_{in}$  and the output voltage  $V_x$  of the correction circuit can be expressed by Formula 9 and Formula 10, respectively.

## 12

[Formula 9]

$$V_{in} = \frac{R_m + R_{on}}{R_{pu} + R_m + R_{on}} \cdot V_p + \frac{R_{pu}}{R_{pu} + R_m + R_{on}} \cdot V_n \quad (9)$$

[Formula 10]

$$V_x = \frac{R_{on}}{R_{pu} + R_m + R_{on}} \cdot V_p + \frac{R_{pu} + R_m}{R_{pu} + R_m + R_{on}} \cdot V_n \quad (10)$$

Formula 11 can be obtained from Formula 8 to Formula 10.

[Formula 11]

$$n = \frac{R_m}{R_{pu}} \cdot N \Rightarrow R_m = \frac{n}{N} \cdot R_{pu} \quad (11)$$

According to Formula 11, the measurement resistance  $R_m$  can be measured from the count number  $N$  in the period  $t_1$ , the count number  $n$  in the period  $t_2$ , and the reference resistance  $R_{pu}$ . A resistance value of the measurement resistance  $R_m$  can be measured without being affected by the  $R_{on}$  that is the on-resistance of the selector switches 4A, 4B, and 4C also with the formula. Such a calculation may be performed using an arithmetic unit that is a microcomputer (MCU) etc.

Here, in the case where the measurement resistance  $R_m$  is set to  $400\Omega$  and the on-resistance  $R_{on}$  of the selector switches 4A, 4B, and 4C is set to  $100\Omega$ , the measurement result according to the related art of FIG. 9 and FIG. 10 and the measurement result according to the technology of FIG. 1 are compared concretely.

Parameters are set to  $V_p = 3.6$  V,  $V_n = 2.4$  V, and  $R_{pu} = 2$  k $\Omega$  as known values.

[Formula 12]

$$\left. \begin{aligned} R_m + R_{on} &= \frac{V_n - V_{in}}{V_{in} - V_p} \cdot R_{pu} \\ V_{in} &= \frac{R_m + R_{on}}{R_{pu} + R_m + R_{on}} \cdot V_p + \frac{R_{pu}}{R_{pu} + R_m + R_{on}} \cdot V_n \end{aligned} \right\} \quad (12)$$

From Formula 12 in the related art, the followings become to be set:  $V_{in} = 2.64$  V and  $R_m + R_{on} = 500\Omega$ . In a practical use, since the value of the on-resistance of the selector switch is unknown, the resistance value of the measurement resistance  $R_m$  will be measured to be a value larger than an actual value.

In contrast to this, in the case where the measurement resistance  $R_m$  is found by the method explained in FIG. 1, since  $V_x$  becomes  $V_x = 2.448$  V by Formula 13 and  $n/N = 0.2$  is found,  $R_m$  can be measured correctly as  $R_m = 0.2 \times 2$  k $\Omega = 400\Omega$ .

[Formula 13]

$$\left. \begin{aligned} R_m &= \frac{n}{N} \cdot R_{pu} \\ \frac{n}{N} &= \frac{V_{in} - V_x}{V_p - V_{in}} \\ V_x &= \frac{R_{on}}{R_{pu} + R_m + R_{on}} \cdot V_p + \frac{R_{pu} + R_m}{R_{pu} + R_m + R_{on}} \cdot V_n \end{aligned} \right\} \quad (13)$$

13

As is clear from the above, the influence of the on-resistance  $R_{on}$  of the selector switches 4A, 4B, and 4C is given to neither the first integral operation nor the second integral operation performed by the Miller integrating circuit 12, and it is possible to suppress the detection accuracy of the measurement resistance  $R_m$  from decreasing caused by the on-resistance  $R_{on}$  of the selector switches 4A, 4B, and 4C.

It is conceivable that the measurement resistance  $R_m$  is used in a range of resistance value of  $20\Omega$  to  $400\Omega$ . At this time, in the related art, since the on-resistance of the selector switch will be added to the measurement resistance as it is, it turns out that in the case where the resistance value of the measurement resistance  $R_m$  is small, the measurement resistance  $R_m$  is susceptible to be affected by the on-resistance of the selector switch as is illustrated in FIG. 11. Moreover, with a technology using a relative ratio like the double integral ADC, it is difficult to perform an accurate resistance measurement because measurement accuracy affected by addition of the on-resistance of the selector switch differs depending on the measurement resistance value  $R_m$ .

Therefore, in the above-mentioned embodiment, it is possible to measure the resistance value of the measurement resistance with high precision.

FIG. 3 shows another example of the correction circuit 7. The correction circuit shown in FIG. 3 is comprised with the use of a switched capacitor while the buffer amplifier by a voltage follower amplifier is ceased to be used. That is, the correction circuit 7 has an operational amplifier 41 that receives the second voltage  $V_n$  at its noninverting input terminal (+) and to which one capacitance electrode of an input capacitance 40 is bound at its inverting input terminal (-). A feedback switch 42 that makes feedback coupling of an output terminal of the operational amplifier 41 to the inverting input terminal (-) and a feedback capacitance 43 that is coupled to the feedback switch 42 in parallel are provided. The feedback switch 42 is switch-controlled by a control signal S1. An input switch 44 that is switch-controlled by the control signal S1 in phase with the feedback switch 42 is arranged and this input switch 44 applies the voltage  $V_{in}$  of the first node N1 to the other capacitance electrode of the input capacitance 40 in the ON state. Moreover, an input switch 45 that is switch-controlled by a control signal S2 in reverse phase with the input switch 44 is arranged, and the input switch 45 applies the voltage  $V_b$  of the second nodes N2 to the other capacitance electrode of the input capacitance 40 in the ON state.

FIG. 4 illustrates an operation timing of the correction circuit 7 of FIG. 3. The control signals S1, S2 turn on the corresponding switches 43, 44, and 45 with their high levels (High), and turn off the corresponding switches 43, 44, and 45 with their low levels (Low). First, S1 is set to the high level and S2 is set to the low level, which makes the feedback capacitance 43 reset, and an output  $V_x$  of the operational amplifier 41 is initialized to  $V_n$ . After this, the correction voltage of  $V_x = V_n + (V_{in} - V_b)$  can be generated by the control signals S1, S2 being reversed.

Although the correction circuit 7 of FIG. 3 can be reduced in circuit scale compared with FIG. 1 by an amount that it does not require the buffer amplifiers 22, 23, it must be taken care that a time until the correction voltage  $V_x$  is decided becomes long compared with FIG. 1.

FIG. 5 shows another example of the comparator circuit in the double integral ADC 1. Here, the comparator circuit uses one hysteresis comparator 14 and makes it possible to compare the correction voltage  $V_x$  selected by a selective switch 50A or the first voltage  $V_p$  selected by a selective switch 50B with an output of the integrating circuit 12. Selection of the

14

selective switches 50A, 50B is controlled by the control signal 31 in the same mode as that of the switches 10A, 10B. That is, the switches 10B, 50B and the switches 10A, 50B are switch controlled complementarily.

Thereby, the number of hysteresis comparators can be reduced by half.

<<Second Embodiment of Second Semiconductor Device>>

FIG. 6 shows a second example of a semiconductor device having the double integral analog-digital conversion circuit. Although a semiconductor device 1A shown in the figure is especially not limited, it is formed over one semiconductor substrate as of single crystal silicon by a known CMOS integrated circuit manufacturing technology. Points of difference from FIG. 1 are that a double integral ADC 6A for inputting therein the second voltage of the second nodes N2A, N2B, and N2C as the input voltage  $V_{in}$  is adopted and that a correction circuit 7A for generating the correction voltage  $V_x$  by adding the on-resistance  $R_{on}$  to the first voltage  $V_p$  is adopted. The semiconductor device 1A will be described below focusing on the points of difference.

In order that the semiconductor device 1A configures the input circuit 2 through the above-mentioned reference resistance  $R_{pu}$  and the multiple measurement resistances  $R_m$ , the semiconductor device 1A has: a first node N1 coupled to the first voltage  $V_p$  through the reference resistance  $R_{pu}$ ; the multiple second nodes N2A, N2B, and N2C coupled to the second voltage  $V_n$  through the measurement resistances  $R_m$ , respectively; and the multiple selector switches 4A, 4B, and 4C for selecting one of the second nodes N2A, N2B, and N2C to be coupled to the first node. On-resistance of the selector switches 4A, 4B, and 4C is designated as  $R_{on}$ . By any one of the selector switches 4A, 4B, and 4C being turned on, a current path extending from the first voltage  $V_p$  to the second voltage  $V_n$  is formed, and the voltage of the first node N1 and the voltage of the second nodes N2i both of which are formed by resistance voltage division are shown in the figure as  $V_c$  and  $V_{in}$ , respectively. The selective switches 5A, 5B, and 5C for inputting the voltages of the selected selector switches 4A, 4B, and 4C on sides of the second nodes N2A, N2B, and N2C in response to the on-operation of the selector switches 4A, 4B, and 4C are arranged. The selector switches 4A, 4B, and 4C and the selective switches 5A, 5B, and 5C form a detection channel switching circuit 3A. Although being especially not limited, the switch control for the detection channel switching circuit 3A is performed by the control signal 30 outputted from the control circuit 16 or is performed by another logic circuit whose illustration is omitted. Incidentally, the first voltage  $V_p$  and the second voltage  $V_n$  may be voltages generated by a power supply circuit of the semiconductor device 1, or may be voltages given from the outside of the semiconductor device 1.

The semiconductor device 1A has the double integral analog-digital conversion circuit (also described as the double integral ADC) 6A and the correction circuit 7A.

The correction circuit 7A generates a voltage obtained by subtracting a voltage between the second node N2A, N2B, or N2C selected by the selector switches 4A, 4B, and 4C and the first node N1 from the first voltage  $V_p$  as the correction voltage  $V_x$ . For example, in FIG. 6, the correction circuit 7 has: the first buffer amplifier 22 that receives a voltage  $V_c$  of the first node N1; the second buffer amplifier 23 that receives the voltage  $V_{in}$  of the second node N2A, N2B, or N2C selected by the selector switches 4A, 4B, and 4C through the selective switch 5A, 5B, or 5C; and the differential amplifier 24 that forms a voltage obtained by adding the first voltage  $V_p$  to a difference voltage of the output of the first buffer amplifier 22 with respect to the output of the second buffer amplifier

15

23 as the correction voltage  $V_x$ . The resistances 25, 26, 27, and 28 are for gain adjustment.

The double integral ADC 6A is for finding the first integral time  $t_1$  elapsed when the difference voltage of the correction voltage  $V_x$  with respect to the voltage  $V_{in}$  of the second nodes N2A, N2B, and N2C is integrated to the second voltage  $V_x$  and the second integral time  $t_2$  elapsed when a difference voltage of the second voltage  $V_n$  with respect to the voltage  $V_{in}$  of the second nodes N2A, N2B, and N2C is integrated to the correction voltage  $V_x$ . Further in detail, the double integral ADC 6A has, in its first stage, the Miller integrating circuit 12 that receives the voltage  $V_{in}$  at its noninverting input terminal (+) and receives the second voltage  $V_n$  selected by the switches 10A, 10B or the correction voltage  $V_x$  at its inverting input terminal (-). 13 is the integral capacity (C) and 11 is the integral resistor (R). Selection of the switches 10A, 10B is controlled by the control signal 31 outputted from the control circuit 16. The Miller integrating circuit 12 performs the first integral operation of integrating the difference voltage of the correction voltage  $V_x$  with respect to the voltage  $V_{in}$  and the second integral operation of integrating the difference voltage of the second voltage  $V_n$  with respect to the voltage  $V_{in}$ . The hysteresis comparator 14A that generates the detection pulse (the first detection signal) 15A when the integral output of the Miller integrating circuit 12 reaches the first voltage  $V_n$  in the first integral operation and the hysteresis comparator 14 that generates the detection pulse (the second detection signal) 15B when the output of the Miller integrating circuit 12 reaches the correction voltage  $V_x$  in the second integral operation are arranged as the comparator circuits.

The first detection signal 15A and the second detection signal 15B are supplied to the control circuit 16. The control circuit 16 operates using the clock signal CK outputted from the clock generation circuit (CPG) 19 as a reference clock, and performs control of the counter 20 for counting the clock signal CK, selection control of the selective switches 10A, 10B, etc. The control circuit 16 controls operations that accumulates, in the register 17, the first count value N counted by the counter 20 in a period spanning from making the integrating circuit 12 start the first integral operation by selecting the correction voltage  $V_x$  with the selective switch 10B until the first detection signal 14A is generated, and further accumulates, in the register 18, the second count value n counted by the counter 20 in a period spanning from making the integrating circuit 12 start the second integral operation by selecting the first voltage  $V_p$  with the selective switch 10A until the second detection signal 14B is generated.

According to a configuration of FIG. 6, when one of the selector switches 4A, 4B, and 4C is selected, a current flowing into the second voltage  $V_n$  from the first voltage  $V_p$  is designated as I. At this time, the voltage  $V_c$  of the first node N1 is a sum ( $V_c = V_n + IR_m + IR_{on}$ ) of the second voltage  $V_n$ , the drop voltage  $IR_m$  by the measurement resistance  $R_m$ , and the drop voltage  $IR_{on}$  by the on-resistance of the selector switch. Moreover, the correction voltage  $V_x$  is a difference ( $V_x = V_p - IR_{on}$ ) between the first voltage  $V_p$  and the drop voltage  $IR_{on}$  by the selector switch. The first voltage  $V_p$  can be expressed as a sum ( $V_p = V_n + IR_m + IR_{on} + IR_{pu}$ ) of the second voltage  $V_n$ , the drop voltage  $IR_m$  by the measurement resistance  $R_m$ , the drop voltage  $IR_{on}$  by the selector switch, and the drop voltage  $IR_{pu}$  by the reference resistance  $R_{pu}$ . Therefore, the integral time  $t_1$  of the first integral operation elapsed when the difference voltage ( $V_{in} - V_x = -IR_{pu}$ ) of the correction voltage  $V_x$  to the voltage  $V_{in}$  of the second nodes N2A, N2B, and N2C is integrated to the first voltage  $V_n$  does not include the component of the on-resistance  $R_{on}$  of the selector switches 4A, 4B,

16

and 4C. On the other hand, similarly, the second integral time  $t_2$  of the second integral operation when the difference voltage ( $V_{in} - V_n = IR_m$ ) of the second voltage  $V_n$  to the voltage  $V_{in}$  of the second nodes N2A, N2B, and N2C is integrated to the correction voltage  $V_x$  does not include the component of the on-resistance  $R_{on}$  of the selector switches 4A, 4B, and 4C. Therefore, the voltage drop by the on-resistance  $R_{on}$  of the selector switches 4A, 4B, and 4C affects neither the first integral operation nor the second integral operation performed by the Miller integrating circuit 12. Therefore, since the influence of the on-resistance of the selector switch comes to be consistent between the first integral and the second integral of the double integral, it is possible to suppress the detection accuracy of the measurement resistance from decreasing caused by the on-resistance of the selector switch.

In the circuit configuration of FIG. 6, a relationship corresponding to Formula 8 becomes Formula 14.

[Formula 14]

$$n = \frac{V_{in} - V_n}{V_x - V_{in}} \cdot N \quad (14)$$

Here, the input voltage  $V_{in}$  and the output voltage  $V_x$  of the correction circuit are expressed by Formula 15 and Formula 16, respectively.

[Formula 15]

$$V_{in} = \frac{R_m}{R_{pu} + R_m + R_{on}} \cdot V_p + \frac{R_{pu} + R_{on}}{R_{pu} + R_m + R_{on}} \cdot V_n \quad (15)$$

[Formula 16]

$$V_x = \frac{R_{pu} + R_m}{R_{pu} + R_m + R_{on}} \cdot V_p + \frac{R_{on}}{R_{pu} + R_m + R_{on}} \cdot V_n \quad (16)$$

Formula 17 can be obtained from Formula 14 to Formula 16.

[Formula 17]

$$n = \frac{R_m}{R_{pu}} \cdot N \Rightarrow R_m = \frac{n}{N} \cdot R_{pu} \quad (17)$$

According to Formula 17, the measurement resistance  $R_m$  can be measured from the count number N in the period  $t_1$ , the count number n in the period  $t_2$ , and the reference resistance  $R_{pu}$ . Since the component of the on-resistance  $R_{on}$  of the selector switches 4A, 4B, and 4C is not included in this operation, the resistance value of the measurement resistance can always be acquired with high precision regardless of a resistance ratio of the reference resistance  $R_{pu}$  and the measurement resistance  $R_m$ . In order to perform such an operation, what is necessary is just to perform it using an arithmetic unit such as a microcomputer (MCU).

Since other points are the same as those of FIG. 1, their detailed explanations are omitted.

FIG. 7 shows another example of the correction circuit 7A. It is comprised with the use of a switched capacitor like FIG. 3. That is, the correction circuit 7A has the operational ampli-

17

fier 41 that receives the first voltage  $V_p$  at its noninverting input terminal (+) and to which the one capacitance electrode of the input capacitance 40 is bound at its inverting input terminal (-). The feedback switch 42 that makes feedback coupling of the output terminal of the operational amplifier 41 to the inverting input terminal (-) and the feedback capacitance 43 that is coupled to the feedback switch 42 in parallel are provided. The feedback switch 42 is switch-controlled by the control signal S1. The input switch 44 that is switch-controlled by the control signal S1 in phase with the feedback switch 42 is arranged, and this input switch 44 applies the voltage  $V_c$  of the first node N1 to the other capacitance electrode of the input capacitance 40 in the ON state. Moreover, the input switch 45 that is switch-controlled by the control signal S2 in reverse phase with the input switch 44 is arranged, and the input switch 45 applies the voltage  $V_{in}$  of the second nodes N2A, N2B, and N2C to the other capacitance electrode of the input capacitance 40 in the ON state.

Although an operation timing is not illustrated in particular, like FIG. 4, the control signals S1, S2 turn on the corresponding switches 43, 44, and 45 with their high levels (High), and turn off the corresponding switches 43, 44, and 45 with their low levels (Low). First, S1 is set to the high level and S2 is set to the low level, which resets the feedback capacitance 43 and initializes the output  $V_x$  of the operational amplifier 41 to  $V_p$ . After this, the correction voltage of  $V_x = V_p + (V_{in} - V_c)$  can be generated by the control signals S1, S2 being reversed.

<<One Embodiment of Electronic Control Device>>

FIG. 8 illustrates an engine control system mounted on an automobile as one example of the electronic control device. A control object of an engine control system 60 is an engine 64, and the system performs engine control of a mixing ratio of gasoline and air, ignition timing, etc. by measuring temperatures of engine exhaust, inspiration, coolant, etc. The engine control system 60 has the semiconductor device 1 (1A) comprised of the semiconductor circuit 1(1A) and the input circuit 2 (2A). A configuration of a temperature sensor 61 is as explained based on FIG. 1, FIG. 6, etc. The measurement resistance  $R_m$  is, for example, a thermistor for engine exhaust, a thermistor for engine inspiration, a thermistor for engine coolant, etc. A microcomputer 63 calculates the resistance value of the measurement resistance  $R_m$  based on Formula 11, Formula 17, etc., generates a control signal 65 using the calculation result, and performs engine control with this.

For delivery of the count values N, n by the first integral operation and the second integral operation, interruption is used, for example. Specifically, when the count values N, n are acquired in the four registers 17, 18 by the temperature sensor 61 performing the above-mentioned first integral operation and second integral operation periodically using respective measurement resistances, the control circuit outputs an interrupt request signal IRQ to the microcomputer 63. In response to the interrupt request, the microcomputer 63 starts an arithmetic processing routine of the measurement resistance. By this, the resistance value of the measurement resistance  $R_m$  is calculated and control of the automobile engine is performed according to the calculation result. Since the count values N, n can be measured with high precision as described above, it is possible to acquire the resistance value with high precision for the measurement resistance  $R_m$ . That is, it is possible to perform the engine control, such as of temperature of the engine etc. with high precision.

The measurement resistance is not limited to the thermistor used for thermometry. The measurement resistance may be the photoconductive cell used for photodetection. A CDS photoconductive cell used for an optical sensor has a charac-

18

teristic that when it is bright, its resistance becomes low, and when it is dark, the resistance becomes high. Therefore, it becomes possible to detect brightness of light with a resistance value acquired by the double integral ADC. The measurement resistance may be a resistance element used for gas concentration measurement. The gas concentration sensor also exhibits rise and fall of its resistance value depending on a concentration of gas, which makes it possible to detect the concentration with the resistance value.

The present invention is not limited to the above-mentioned embodiments and it goes without saying that it can be modified variously without deviating from its gist.

For example, the resistance used for the input circuit of the double integral ADC is not limited to the resistance element, but it can be comprised of an on-resistance of a transistor, a switched capacitor, or the like. The measurement resistance is not limited to the thermistor for thermometry, the photoconductive cell of the optical sensor, and the resistance element of the gas concentration sensor, but can be modified suitably. Moreover, in each of FIG. 1 and FIG. 6, the semiconductor device is also configurable with a voltage polarity being reversed as a whole. The electronic control device is widely applicable to other in-vehicle systems, industrial facilities, household systems, etc., not being limited to the engine control system.

What is claimed is:

1. A semiconductor device, comprising:

a first node coupled to a first voltage through a reference resistance;

a plurality of second nodes coupled to a second voltage through measurement resistances;

a plurality of selector switches for selecting the second node to be coupled to the first node;

a correction circuit that generates a voltage obtained by adding the second voltage to a voltage between the second node selected by the selector switches and the first node as a correction voltage; and

a double integral analog-digital conversion circuit that finds a first integral time elapsed when a difference voltage of the correction voltage with respect to a voltage of the first node is integrated to the first voltage and a second integral time elapsed when a difference voltage of the first voltage with respect to the voltage of the first node is integrated to the correction voltage.

2. The semiconductor device according to claim 1,

wherein the double integral analog-digital conversion circuit has:

an integrating circuit that performs a first integral operation of integrating the difference voltage of the correction voltage with respect to the voltage of the first node and a second integral operation of integrating the difference voltage of the first voltage with respect to the voltage of the first node;

a detection circuit that generates a first detection signal when an integral output of the integrating circuit reaches the first voltage in the first integral operation and generates a second detection signal when the integral output of the integrating circuit reaches the correction voltage in the second integral operation;

a counter for counting a clock signal; and

a control circuit that acquires a first count value by the counter from when the first count operation is started by the integrating circuit until the first detection signal is generated, and a second count value by the counter from when the second count operation is started thereby until the second detection signal is generated.

## 19

3. The semiconductor device according to claim 2,  
wherein the integrating circuit is a Miller integrating circuit  
that receives the voltage of the first node at its noninvert-  
ing input terminal and receives selectively the first volt-  
age or the correction voltage at its inverting input termi-  
nal. 5
4. The semiconductor device according to claim 1,  
wherein the correction circuit has:  
a first buffer amplifier for receiving the voltage of the first  
node; 10  
a second buffer amplifier for receiving a voltage of the  
second node selected by the selector switches; and  
a differential amplifier that forms a voltage obtained by  
adding the second voltage to a difference voltage of an  
output of the second buffer amplifier with respect to an  
output of the first buffer amplifier as the correction volt-  
age. 15
5. The semiconductor device according to claim 1,  
wherein the correction circuit includes: 20  
an operational amplifier that receives the second voltage at  
its noninverting input terminal and to which one capaci-  
tance electrode of an input capacitance is bound at its  
inverting input terminal;  
a first switch that makes feedback coupling of an output 25  
terminal of the operational amplifier to the inverting  
input terminal;  
a feedback capacitance that is coupled to the first switch in  
parallel;  
a second switch that is switch-controlled in phase with the 30  
first switch and applies the voltage of the first node to the  
other capacitance electrode of the input capacitance in  
the ON state; and  
a third switch that is switch-controlled in reverse phase  
with the first switch and applies a voltage of the second 35  
nodes to the other capacitance electrode of the input  
capacitance in the ON state.
6. The semiconductor device according to claim 1,  
wherein the first node and the second nodes are external  
terminals. 40
7. A semiconductor device, comprising:  
a first node coupled to a first voltage through a reference  
resistance;  
a plurality of second nodes coupled to a second voltage  
through measurement resistances; 45  
a plurality of selector switches for selecting the second  
node to be coupled to the first node;  
a correction circuit that generates a voltage obtained by  
subtracting a voltage between the second node selected  
by the selector switches and the first node from the first 50  
voltage as a correction voltage; and  
a double integral analog-digital conversion circuit that  
finds a first integral time elapsed when a difference volt-  
age of the correction voltage with respect to a voltage of  
the second nodes is integrated to the second voltage and 55  
a second integral time elapsed when a difference voltage  
of the second voltage with respect to the voltage of the  
second nodes is integrated to the correction voltage.
8. The semiconductor device according to claim 7,  
wherein the double integral analog-digital conversion cir-  
cuit has: 60  
an integrating circuit that performs a first integral operation  
of integrating the difference voltage of the correction  
voltage with respect to the voltage of the second nodes  
and a second integral operation of integrating the differ-  
ence voltage of the second voltage with respect to the  
voltage of the second nodes; 65

## 20

- a detection circuit that generates a first detection signal  
when an integral output of the integrating circuit reaches  
the second voltage in the first integral operation and  
generates a second detection signal when an integral  
output of the integrating circuit reaches the correction  
voltage in the second integral operation;  
a counter for counting a clock signal; and  
a control circuit that acquires a first count value by the  
counter from when the first integral operation is started  
by the integrating circuit until the first detection signal is  
generated and a second count value by the counter from  
when the second integral operation is started by the  
integrating circuit until the second detection signal is  
generated.
9. The semiconductor device according to claim 8,  
wherein the integrating circuit is a Miller integrating circuit  
that receives the voltage of the second nodes at its non-  
inverting input terminal and receives selectively the sec-  
ond voltage or the correction voltage at its inverting  
input terminal.
10. The semiconductor device according to claim 7,  
wherein the correction circuit has:  
a first buffer amplifier for receiving a voltage of the first  
node;  
a second buffer amplifier for receiving the voltage of the  
second node selected by the selector switches; and  
a differential amplifier that forms a voltage obtained by  
subtracting a difference voltage of an output of the sec-  
ond buffer amplifier with respect to an output of the first  
buffer amplifier from the first voltage as the correction  
voltage.
11. The semiconductor device according to claim 7,  
wherein the correction circuit includes:  
an operational amplifier that receives the first voltage at its  
noninverting input terminal and to which one capaci-  
tance electrode of an input capacitance is bound at its  
inverting input terminal;  
a first switch that makes feedback coupling of an output  
terminal of the operational amplifier to the inverting  
input terminal;  
a feedback capacitance that is coupled to the first switch in  
parallel;  
a second switch that is switch-controlled in phase with the  
first switch and applies the voltage of the first node to the  
other capacitance electrode of the input capacitance in  
the ON state; and  
a third switch that is switch-controlled in reverse phase  
with the first switch and applies the voltage of the second  
nodes to the other capacitance electrode of the input  
capacitance in the ON state.
12. The semiconductor device according to claim 7,  
wherein the first node and the second nodes are external  
terminals.
13. An electronic control device, comprising:  
a plurality of measurement resistances provided in a con-  
trol object apparatus;  
a reference resistance;  
a first node coupled to a first voltage through the reference  
resistance;  
a plurality of second nodes coupled to a second voltage  
through the measurement resistances;  
a plurality of selector switches for selecting the second  
node to be coupled to the first node;  
a correction circuit for generating a voltage obtained by  
adding the second voltage to a voltage between the sec-  
ond node selected by the selector switches and the first  
node as a correction voltage;

## 21

- a double integral analog-digital conversion circuit that finds a first integral time elapsed when a difference voltage of the correction voltage with respect to a voltage of the first node is integrated to the first voltage and a second integral time elapsed when a difference voltage of the first voltage with respect to the voltage of the first node is integrated to the correction voltage; and
- a control part that inputs therein the first integral time and the second integral time, calculates a value obtained by multiplying a rate of the first integral time to the second integral time by a resistance value of the reference resistance as a resistance value of the measurement resistance, and controls the control object apparatus based on the calculation result.
14. The electronic control device according to claim 13, wherein the measurement resistance is a thermistor used for thermometry.
15. The electronic control device according to claim 14, wherein the control object apparatus is an automobile engine.
16. The electronic control device according to claim 13, wherein the measurement resistance is a photoconductive cell used for photodetection.
17. The electronic control device according to claim 13, wherein the measurement resistance is a resistance element used for gas concentration measurement.

## 22

18. An electronic control circuit, comprising:
- a plurality of measurement resistances provided in a control object apparatus;
  - a reference resistance;
  - a first node coupled to a first voltage through the reference resistance;
  - a plurality of second nodes coupled to a second voltage through the measurement resistances;
  - a plurality of selector switches for selecting the second node to be coupled to the first node;
  - a correction circuit that generates a voltage obtained by subtracting a voltage between the second node selected by the selector switches and the first node from the first voltage as a correction voltage;
  - a double integral analog-digital conversion circuit that finds a first integral time elapsed when a difference voltage of the correction voltage with respect to the voltage of the second nodes is integrated to the second voltage and a second integral time elapsed when a difference voltage of the second voltage with respect to the voltage of the second nodes is integrated to the correction voltage; and
  - a control part that inputs therein the first integral time and the second integral time, calculates a value obtained by multiplexing a ratio of the first integral time to the second integral time by a resistance value of the reference voltage, and controls the control object apparatus based on the calculation result.

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